PATENT ABSTRACTS OF JAPAN

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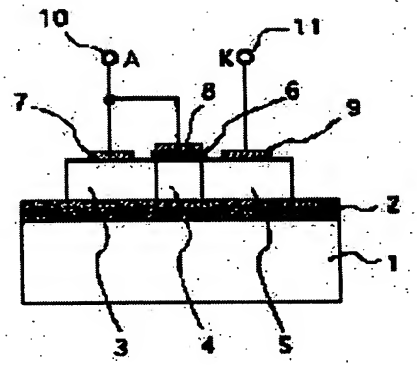
(54) RECTIFIER DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce a forward voltage such that a forward current starts flowing and reduce a reverse voltage, by commonly connecting a gate electrode with a first wiring metal layer to form an anode terminal and causing a second wiring metal layer to be a cathode terminal.



SOLUTION: By applying a voltage so that an anode terminal 10 is positively charged and a cathode terminal 11 is negatively charged, a channel is formed on the interface of a second semiconductor region 4 with a gate insulating film 6. As a result, a current path is formed from a first semiconductor region 3 via the channel to a third semiconductor region 5. Conditions for forming the channel are adjustable by physical constants, such as, the density of impurity in the second semiconductor region 4, the thickness of the gate insulating film 6, and the type of a gate electrode 8. The constants may be so selected that the channel is formed at a forward voltage between anode and cathode being not lower than 0V. If a lower voltage is applied to the anode terminal 10 than the voltage applied to the cathode terminal 11, no channel is formed in the second semiconductor region 4.

LEGAL STATUS

[Date of request for examination]

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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] A rectifying device characterized by using a metal layer for wiring of the above 2nd as a cathode terminal while having the following, making common connection of the above-mentioned gate electrode and the metal layer for wiring of the above 1st and considering as an anode terminal. A support substrate which has a pad insulating layer in a 1st principal plane side A single crystal semiconductor film which has the 3rd semiconductor region of the 1st electric conduction form which does not adjoin the 1st semiconductor region of the above while adjoining the 1st semiconductor region of the 1st electric conduction form, and this 1st semiconductor region and adjoining the 2nd semiconductor region and this 2nd semiconductor region of an electric conduction form opposite to the 1st electric conduction form, and was prepared in the above-mentioned insulating-layer upper surface [2nd] A gate electrode formed in the surface of the 2nd semiconductor region of the above by intervening in a gate insulator layer The 1st metal layer for wiring by which ohmic contact was carried out to the surface of the 1st semiconductor region of the above, and the 2nd metal layer for wiring by which ohmic contact was carried out to the surface of the 3rd semiconductor region of the above
[Claim 2] A rectifying device characterized by using a metal layer for wiring of the above 2nd as a cathode terminal while having the following, making common connection of the above-mentioned gate electrode and the metal layer for wiring of the above 1st and considering as an anode terminal. A support substrate which has a pad insulating layer in a 1st principal plane side A single crystal semiconductor film which does not adjoin the 1st semiconductor region of the above while adjoining the 1st semiconductor region and this 1st semiconductor region and adjoining the 2nd semiconductor region and this 2nd semiconductor region of low high impurity concentration compared with this 1st semiconductor region in the same electric conduction form as this 1st semiconductor region, but has the 3rd semiconductor region of high high impurity concentration compared with the 2nd semiconductor region of the above in the same electric conduction form as the 1st semiconductor region of the above, and was prepared on the above-mentioned insulating layer A gate electrode formed in the surface of the 2nd semiconductor region of the above by intervening in a gate insulator layer The 1st metal layer for wiring by which ohmic contact was carried out to the surface of the 1st semiconductor region of the above, and the 2nd metal layer for wiring by which ohmic contact was carried out to the surface of the 3rd semiconductor region of the above

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] This invention relates to the rectifying device which made low forward voltage to which the rectifying device used for switching power supplies, such as a DC-DC converter, etc. is started, especially forward current begins to flow, and made the reverse current small.
[0002]
[Description of the Prior Art] The structure of the Schottky barrier diode generally used as a rectifying device is shown in drawing 5 . For the semiconductor region of low high impurity concentration, and 23, as for the metal layer for wiring, and 26, in this drawing, a barrier metal, and 24 and 25 are [21 / a semiconductor substrate and 22 / an anode terminal and 27] cathode terminals. In this example, as for the semiconductor substrate 21 and a semiconductor region 22, the silicon semiconductor of n form is used, for example.
[0003] A dotted line shows the voltage/current characteristic of shot key-ber diode to drawing 2 . When forward voltage (the anode terminal 26 is high potential from the cathode terminal 27) is impressed, in order for forward current to flow, a certain amount of voltage needs to be added. This forward voltage changes with the physical properties of the plane of composition of the barrier metal 23, its barrier metal 23, and a semiconductor region 22, and is about [0.3-1.0V] magnitude in usual. When reverse voltage (the anode terminal 26 is low voltage from the cathode terminal 27) is impressed, the reverse current of a Schottky barrier diode is large, and has forward voltage and the relation of a trade-off.
[0004]
[Problem(s) to be Solved by the Invention] Generally, in order to reduce the loss in a rectifying device, it is necessary to reduce a forward voltage drop. The problem of becoming large relatively and becoming the failure of low-battery-izing has loss according to a rectifying device in case output voltage of switching power supplies, such as a DC-DC converter which supplies current, is especially low-battery-ized in order to respond to this, since progress of low-battery-izing of operating voltage is remarkable in a microprocessor etc. However, in a Schottky barrier diode, since the reverse current increased when the forward voltage drop was made small based on the above-mentioned request, there was a problem that low-loss-izing was difficult.
[0005] The purpose of this invention also reduces a reverse current with reduction of the forward voltage to which forward current begins to flow, and uses as an offer plug the rectifying device which has improved the opposite property made conventionally difficult.
[0006]
[Means for Solving the Problem] For this reason, a support substrate with which the 1st invention has a pad insulating layer in a 1st principal plane side, The 1st semiconductor region of the 1st electric conduction form and this 1st semiconductor region are adjoined. The 2nd semiconductor region of the 2nd electric conduction form opposite to the 1st electric conduction form, And a single crystal semiconductor film which has the 3rd semiconductor region of the 1st electric conduction form which

does not adjoin the 1st semiconductor region of the above while adjoining this 2nd semiconductor region, and was prepared in the above-mentioned insulating-layer upper surface, A gate electrode formed in the surface of the 2nd semiconductor region of the above by intervening in a gate insulator layer, The 1st metal layer for wiring by which ohmic contact was carried out to the surface of the 1st semiconductor region of the above, While providing the 2nd metal layer for wiring by which ohmic contact was carried out to the surface of the 3rd semiconductor region of the above, making common connection of the above-mentioned gate electrode and the metal layer for wiring of the above 1st and considering as an anode terminal It constituted as a rectifying device characterized by using a metal layer for wiring of the above 2nd as a cathode terminal.

[0007] A support substrate with which the 2nd invention has a pad insulating layer in a 1st principal plane side, and the 1st semiconductor region, This 1st semiconductor region is adjoined and it compares with this 1st semiconductor region in the same electric conduction form as this 1st semiconductor region. The 2nd semiconductor region of low high impurity concentration, And while adjoining this 2nd semiconductor region, the 1st semiconductor region of the above is not adjoined. A single crystal semiconductor film which has the 3rd semiconductor region of high high impurity concentration compared with the 2nd semiconductor region of the above in the same electric conduction form as the 1st semiconductor region of the above, and was prepared on the above-mentioned insulating layer, A gate electrode formed in the surface of the 2nd semiconductor region of the above by intervening in a gate insulator layer, The 1st metal layer for wiring by which ohmic contact was carried out to the surface of the 1st semiconductor region of the above, While providing the 2nd metal layer for wiring by which ohmic contact was carried out to the surface of the 3rd semiconductor region of the above, making common connection of the above-mentioned gate electrode and the metal layer for wiring of the above 1st and considering as an anode terminal It constituted as a rectifying device characterized by using a metal layer for wiring of the above 2nd as a cathode terminal.

[0008]

[Embodiment of the Invention]

[Gestalt of the 1st operation] drawing 1 is the cross section of the rectifying device in which the gestalt of operation of the 1st of this invention is shown. In this drawing, it is the pad insulating layer which formed 1 in the support substrate and formed 2 in the upper surface of the support substrate 1. The 1st semiconductor region and 4 continue in a longitudinal direction in the single crystal semiconductor film which the 2nd semiconductor region and 5 are the 3rd semiconductor region, and was respectively formed on the insulating layer 2, adjoin, and 3 is formed. Moreover, the gate insulator layer in which 6 was formed on the upper surface of the 2nd semiconductor region 4, the metal layer for wiring which carried out ohmic contact of 7 to the upper surface of the 1st semiconductor region 3, the gate electrode in which 8 was formed on the upper surface of the gate insulator layer 6, and 9 are the metal layers for wiring which carried out ohmic contact to the upper surface of the 3rd semiconductor region 5. The anode terminal with which 10 made common connection of the metal layer 7 for wiring and the gate electrode 8, and 11 are the cathode terminals which connected the metal layer 9 for wiring.

[0009] As a support substrate 1, silicon, germanium, GaAs, etc. can be used as a single crystal semiconductor film which formed the 1st - the 3rd semiconductor region 3-5 for silicon, sapphire, a diamond, etc. again. Here, it assumes using silicon as the support substrate 1 and semiconductor regions 3-5, and using the SOI (Silicon on Insulator) structure where the thickness of the silicon film of the semiconductor regions 3-5 is 0.1-0.5 micrometers. The 1st semiconductor region 3 and 3rd semiconductor region 5 are n form, and in order to obtain ohmic contact with the metal layers 7 and 9 for wiring, they make high impurity concentration the concentration of the range of 1x1019cm-3-1x1021cm-3. The 2nd semiconductor region 4 is made into low concentration rather than the high impurity concentration of the 1st and 3rd semiconductor region 3 and 5, when making it into p form or n form and making it into n form.

[0010] Now, if the anode terminal 10 impresses voltage E so that positive and the cathode terminal 11 may serve as negative as shown in drawing 3 (forward direction), when the 2nd semiconductor region 4 is p form, an inversion layer is formed in an interface with the gate insulator layer 6 in the 2nd

semiconductor region 4, when it is low-concentration n form, an accumulation layer will be formed, and this inversion layer or accumulation layer will serve as a channel. Consequently, between the 1st - the 3rd semiconductor region 3-5 is the same electric conduction form, and is connected in the 2nd semiconductor region 4 of low resistance. That is, as the current path was formed of the 1st semiconductor region 3 -> channel -> 3rd semiconductor region 5 and it was shown in drawing 3 , it is forward current If. It flows.

[0011] A continuous line shows this voltage/current characteristic to drawing 2 . Forward current If is expressed to the 1st **** of drawing 2 . Physical constants, such as unseasonable object concentration of the 2nd semiconductor region 4, thickness of the gate insulator layer 6, and a class of gate electrode 8, can adjust the formation conditions of the above-mentioned channel, and when the forward direction applied voltage between anode cathodes choose the constant so that a channel may be form more than by 0V; the property that forward current begin to flow from about 0V as showed in drawing 2 can be realize.

[0012] When you make the 2nd semiconductor region 4 into p form, let thickness of 5x1015cm-3 and the gate insulator layer 6 to 50nm, and, specifically, let the gate electrode 8 be n form polish recon for the high impurity concentration of the semiconductor region 4 (p form). Moreover, thickness of 2x1015cm-3 and the gate insulator layer 6 is made to 50nm, and it makes the gate electrode 8 p form polish recon for the high impurity concentration of the semiconductor region 4 (n form), when making the 2nd semiconductor region 4 into n form. The above mentioned property is acquired by doing in this way.

[0013] In this way, it is clarified by drawing 2 rather than the Schottky barrier diode with the forward voltage required for the rectifying device by this invention which is a work function, silicon surface level, etc. of a barrier metal that a forward voltage drop can be reduced.

[0014] On the other hand, drawing 4 explains the case where reverse voltage is impressed. A channel will not be formed in the 2nd semiconductor region 4 if voltage-E (reverse voltage) lower than the cathode terminal 11 is impressed to the anode terminal 10. Namely, since this 2nd semiconductor region 4 is formed by the thin silicon film which used the SOI substrate, a depletion layer occupies the whole region of the 2nd semiconductor region 4, and it will be in a perfect depletion condition. By this, even if reverse voltage is impressed, current is prevented effectively, and it is stopped by only very minute leakage current Ir.

[0015] In addition, when the 2nd semiconductor region 4 is made into p form, inhibition of current is possible even if it does not form perfect depletion with the obstruction of the pn junction formed in this the 2nd semiconductor region 4 (p form) and 3rd semiconductor region 5 (n form). However, since the leakage current of hard flow flows also to pn junction, the current can be more effectively intercepted by forming perfect depletion, as described above.

[0016] The relation between the high impurity concentration which will be in a perfect depletion-ized condition at drawing 6 , and silicon thickness was shown about the case where the 2nd semiconductor region 4 is p form. The case where the 2nd semiconductor region 4 was n form was shown in drawing 7 . The plotted point is observation data. In order to acquire the effect by this invention, it turns out that what is necessary is to make high impurity concentration of the 2nd semiconductor region 4 into the concentration of the range to or less [1x1017cm -] 3 manufacture limit, and just to make silicon thickness into the thickness of the range to hundreds of nm or less manufacture limit.

[0017] The continuous line of the 3rd phenomenon shown in drawing 2 showed reverse voltage/current characteristic. Unlike the Schottky barrier diode with which a reverse current increases, the rectifying device by this invention is only a minute reverse current, and has the property which was very excellent as a rectifying device, so that forward voltage is reduced.

[0018] as explained above, as compared with the Schottky barrier diode currently used conventionally, the rectifying device by this invention can reduce the forward voltage to which forward current begins to flow, and can attain low loss-ization -- in addition, it has the advantage that loss by the reverse current is also very small since the reverse current when impressing reverse voltage is also minute. Reduction of a forward voltage drop has a big advantage in efficient-ization of the switching power supply of business,

such as a microprocessor to which low-battery-ization of operating voltage progresses.
[0019] Even if it takes the configuration which carried out p form of structure which is [the gestalt of other operations] where the rectifying device of this invention was explained with the gestalt of the 1st operation, and n form reversely, it is needless to say that the same operation effect is acquired.
[0020]
[Effect of the Invention] As mentioned above, since it considered as the configuration which connected the gate electrode of the metal-oxide-semiconductor structure on a SOI substrate to the anode terminal according to this invention, current begins to flow from 0V of forward voltage, and a forward voltage drop lower than the forward voltage drop of the Schottky barrier diode currently used from the former can be realized. Moreover, at the time of reverse voltage impression, leakage current can be suppressed to a minute ** value by perfect depletion-ization for the thin silicon membrane structure by SOI. In this way, especially the rectifying device of this invention has the property which was excellent as a rectifying device of the switching power supply of low-power output voltage, and demonstrates a big effect to low loss-ization of switching power supply.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the cross section of the rectifying device in which the gestalt of operation of the 1st of this invention is shown.
[Drawing 2] They are the voltage / current characteristic drawing of a rectifying device.
[Drawing 3] It is operation explanatory drawing at the time of forward voltage impression of the rectifying device of the gestalt of the 1st operation.
[Drawing 4] It is operation explanatory drawing at the time of reverse voltage impression of the rectifying device of the gestalt of the 1st operation.
[Drawing 5] It is the cross section of the conventional Schottky barrier diode.
[Drawing 6] It is property drawing showing the dependency of the high impurity concentration of silicon thickness formed into perfect depletion when making the 2nd semiconductor region into p form.
[Drawing 7] It is property drawing showing the dependency of the high impurity concentration of silicon thickness formed into perfect depletion when making the 2nd semiconductor region into n form.
[Description of Notations]
1: a support substrate, 2:pad insulating layer, and 3: -- the 1st semiconductor region and 4: -- the 2nd semiconductor region and 5: -- the 3rd semiconductor region, 6:gates insulator layer, and 7: -- the metal layer for wiring, 8:gates electrodes, the metal layer for 9:wiring, 10:anode terminal, and 11:cathode terminal. 21: A semiconductor substrate, the semiconductor region of 22:low concentration, 23:barrier metal, 24, the metal layer for 25:wiring, 26:anode terminal, 27 : cathode terminal.

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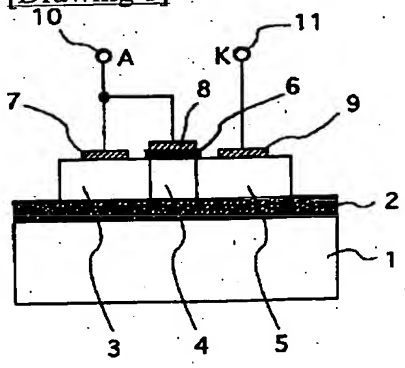
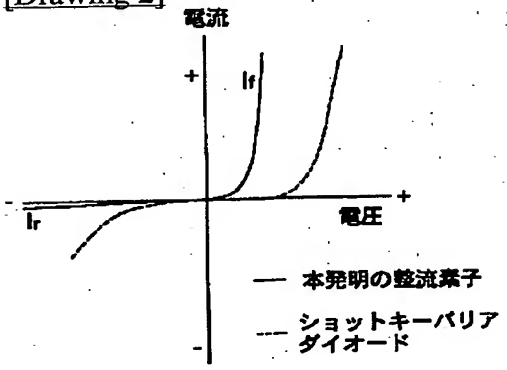
DRAWINGS

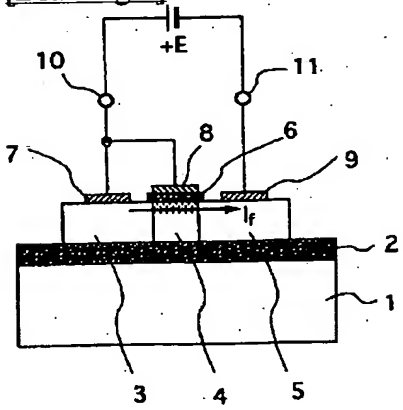
[Drawing 1]



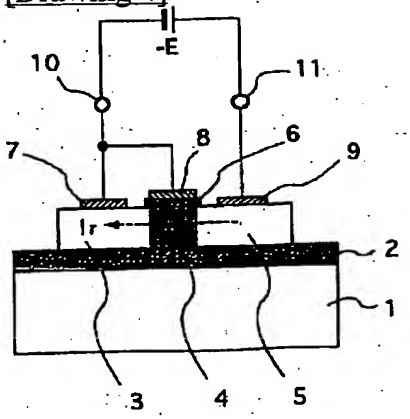
[Drawing 2]



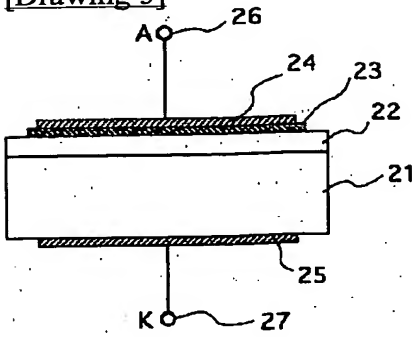
[Drawing 3]



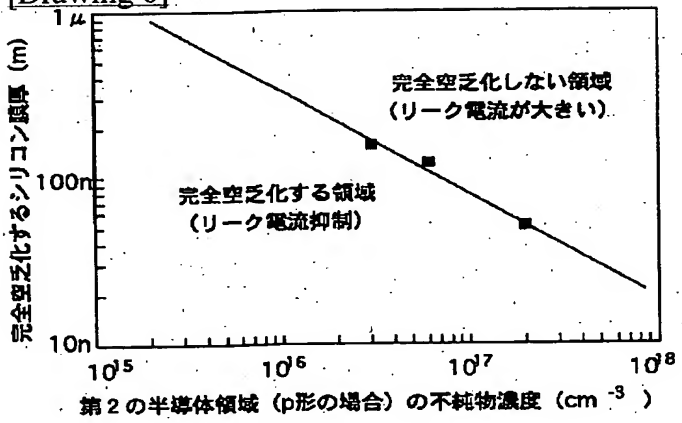
[Drawing 4]



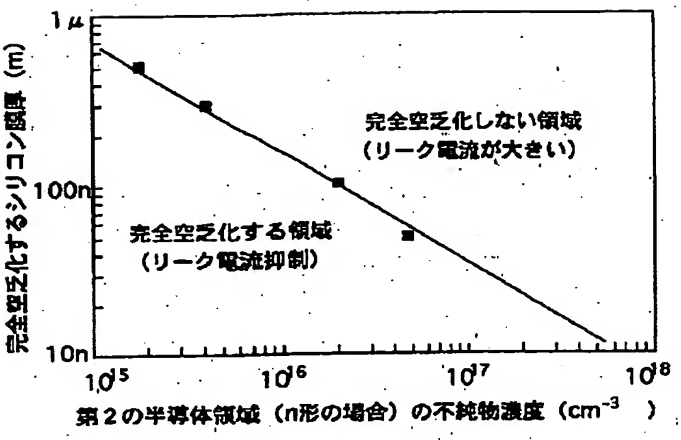
[Drawing 5]



[Drawing 6]



[Drawing 7]



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Ｈ０１Ｌ	29/861		Ｈ０１Ｌ	29/91	Ｌ
	27/12			27/12	Ｚ
	29/872			29/48	Ｆ
	29/786			29/78	６２２

審査請求　未請求　請求項の数２　ＦＤ　（全５頁）

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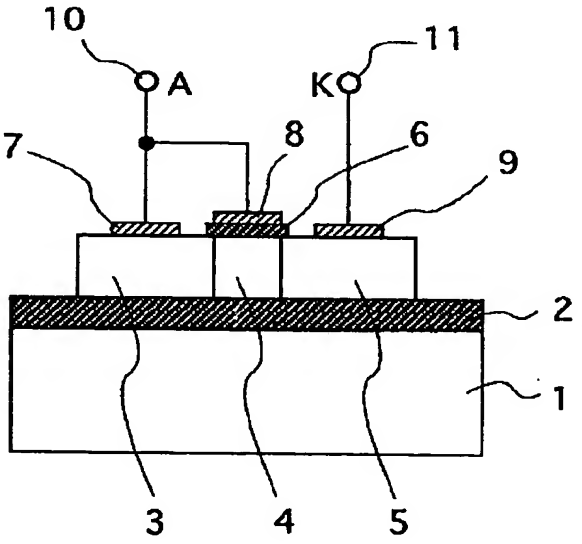
(54)【発明の名称】　整流素子

(57)【要約】

【課題】　順方向電流が流れ始める順方向電圧を低くすると共に、逆方向電流を小さくすること。

【解決手段】　ＳＯＩ基板上のシリコン薄膜内の第１の半導体領域３と第３の半導体領域５をｎ形に、第２の半導体領域２をｐ形にし、半導体領域３とゲート電極８をアノード端子１０に接続し、半導体領域５をカソード端子１１に接続した。



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【特許請求の範囲】

【請求項１】第１の主面側に埋込み絶縁層を有する支持基板と、

第１の導電形の第１の半導体領域、該第１の半導体領域に隣接し第１の導電形と反対の第２の導電形の第２の半導体領域、および該第２の半導体領域に隣接すると共に上記第１の半導体領域と隣接しない第１の導電形の第３の半導体領域を有し、上記絶縁層上面に設けられた単結晶半導体膜と、

上記第２の半導体領域の表面にゲート絶縁膜を介在して形成されたゲート電極と、

上記第１の半導体領域の表面にオーミックコンタクトされた第１の配線用金属層と、

上記第３の半導体領域の表面にオーミックコンタクトされた第２の配線用金属層とを具備し、

上記ゲート電極と上記第１の配線用金属層とを共通接続してアノード端子とすると共に、上記第２の配線用金属層をカソード端子としたことを特徴とする整流素子。

【請求項２】第１の主面側に埋込み絶縁層を有する支持基板と、

第１の半導体領域、該第１の半導体領域に隣接し該第１の半導体領域と同一導電形で該第１の半導体領域に比べ低不純物濃度の第２の半導体領域、および該第２の半導体領域に隣接すると共に上記第１の半導体領域と隣接せず、上記第１の半導体領域と同一導電形で上記第２の半導体領域に比べ高不純物濃度の第３の半導体領域を有し、上記絶縁層上に設けられた単結晶半導体膜と、

上記第２の半導体領域の表面にゲート絶縁膜を介在して形成されたゲート電極と、

上記第１の半導体領域の表面にオーミックコンタクトされた第１の配線用金属層と、

上記第３の半導体領域の表面にオーミックコンタクトされた第２の配線用金属層とを具備し、

上記ゲート電極と上記第１の配線用金属層とを共通接続してアノード端子とすると共に、上記第２の配線用金属層をカソード端子としたことを特徴とする整流素子。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、ＤＣ－ＤＣコンバータ等のスイッチング電源等に用いる整流素子に係り、特に順方向電流が流れ始める順方向電圧を低くし、且つ逆方向電流を小さくした整流素子に関するものである。

【０００２】

【従来の技術】整流素子として一般に用いられているショットキーバリアダイオードの構造を図５に示す。同図において、２１は半導体基板、２２は低不純物濃度の半導体領域、２３はバリア金属、２４、２５は配線用金属層、２６はアノード端子、２７はカソード端子である。この例では、例えば半導体基板２１および半導体領域２２はｎ形のシリコン半導体が使用される。

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【０００３】ショットキーバアダイオードの電圧／電流特性を図２に点線で示す。順方向電圧（アノード端子２６がカソード端子２７よりも高電位）を印加した場合、順方向電流が流れるには、ある程度の電圧が加わる必要がある。この順方向電圧は、バリア金属２３やそのバリア金属２３と半導体領域２２との接合面の物理特性によって変化し、通常では０．３～１．０Ｖ程度の大きさである。逆方向電圧（アノード端子２６がカソード端子２７よりも低電位）を印加した場合、ショットキーバリアダイオードの逆方向電流は大きく、順方向電圧とトレードオフの関係にある。

【０００４】

【発明が解決しようとする課題】一般的に、整流素子における損失を低減するには、順方向電圧降下を低減する必要がある。特に、マイクロプロセッサ等においては動作電圧の低電圧化の進展が著しいので、これに応えるべく、電流を供給するＤＣ－ＤＣコンバータ等のスイッチング電源の出力電圧を低電圧化する際、整流素子による損失は相対的に大きくなり低電圧化の障害になるという問題がある。しかし、ショットキーバリアダイオードでは、上記要請に基づき順方向電圧降下を小さくすると、逆方向電流が増加するので、低損失化が難しいという問題があった。

【０００５】本発明の目的は、順方向電流が流れ始める順方向電圧の低減とともに逆方向電流も低減させ、従来困難とされていた相反する特性を改善した整流素子を提供せんとするものである。

【０００６】

【課題を解決するための手段】このために第１の発明は、第１の主面側に埋込み絶縁層を有する支持基板と、第１の導電形の第１の半導体領域、該第１の半導体領域に隣接し第１の導電形と反対の第２の導電形の第２の半導体領域、および該第２の半導体領域に隣接すると共に上記第１の半導体領域と隣接しない第１の導電形の第３の半導体領域を有し、上記絶縁層上面に設けられた単結晶半導体膜と、上記第２の半導体領域の表面にゲート絶縁膜を介在して形成されたゲート電極と、上記第１の半導体領域の表面にオーミックコンタクトされた第１の配線用金属層と、上記第３の半導体領域の表面にオーミックコンタクトされた第２の配線用金属層とを具備し、上記ゲート電極と上記第１の配線用金属層とを共通接続してアノード端子とすると共に、上記第２の配線用金属層をカソード端子としたことを特徴とする整流素子として構成した。

【０００７】第２の発明は、第１の主面側に埋込み絶縁層を有する支持基板と、第１の半導体領域、該第１の半導体領域に隣接し該第１の半導体領域と同一導電形で該第１の半導体領域に比べ低不純物濃度の第２の半導体領域、および該第２の半導体領域に隣接すると共に上記第１の半導体領域と隣接せず、上記第１の半導体領域と同

一導電形で上記第２の半導体領域に比べ高不純物濃度の第３の半導体領域を有し、上記絶縁層上に設けられた単結晶半導体膜と、上記第２の半導体領域の表面にゲート絶縁膜を介在して形成されたゲート電極と、上記第１の半導体領域の表面にオーミックコンタクトされた第１の配線用金属層と、上記第３の半導体領域の表面にオーミックコンタクトされた第２の配線用金属層とを具備し、上記ゲート電極と上記第１の配線用金属層とを共通接続してアノード端子とすると共に、上記第２の配線用金属層をカソード端子としたことを特徴とする整流素子として構成した。

【０００８】

【発明の実施の形態】

［第１の実施の形態］図１は本発明の第１の実施の形態を示す整流素子の断面図である。同図において、１は支持基板、２はその支持基板１の上面に形成した埋込み絶縁層である。３は第１の半導体領域、４は第２の半導体領域、５は第３の半導体領域であり、各々絶縁層２の上に形成された単結晶半導体膜内に横方向に連続し隣接して形成されている。また、６は第２の半導体領域４の上面に形成したゲート絶縁膜、７は第１の半導体領域３の上面にオーミックコンタクトした配線用金属層、８はゲート絶縁膜６の上面に形成したゲート電極、９は第３の半導体領域５の上面にオーミックコンタクトした配線用金属層である。１０は配線用金属層７とゲート電極８を共通接続したアノード端子、１１は配線用金属層９を接続したカソード端子である。

【０００９】支持基板１としては例えば、シリコン、サファイア、ダイアモンド等を、また第１～第３の半導体領域３～５を形成した単結晶半導体膜としては例えば、シリコン、ゲルマニウム、ＧａＡｓ等が使用できる。ここでは、支持基板１、半導体領域３～５としてシリコンを使用し、その半導体領域３～５のシリコン膜の厚さが０．１～０．５μｍのＳＯＩ（Silicon on Insulator）構造を使用することを想定している。第１の半導体領域３と第３の半導体領域５はｎ形で、配線用金属層７、９とのオーミックコンタクトを得るために不純物濃度を１×10^{19}ｃｍ$^{-3}$～１×10^{21}ｃｍ$^{-3}$の範囲の濃度とする。第２の半導体領域４はｐ形又はｎ形とし、ｎ形とするときは第１、第３の半導体領域３、５の不純物濃度よりも低濃度とする。

【００１０】さて、図３に示すようにアノード端子１０が正、カソード端子１１が負となるように電圧Ｅを印加（順方向）すると、第２の半導体領域４におけるゲート絶縁膜６との界面に、第２の半導体領域４がｐ形のときは反転層が形成され、低濃度のｎ形のときは蓄積層が形成され、この反転層または蓄積層はチャンネルとなる。この結果、第１～第３の半導体領域３～５の間が、同一の導電形で且つ低抵抗の第２の半導体領域４で接続される。すなわち、第１の半導体領域３→チャンネル→第３の半導体領域５により電流経路が形成され、図３に示したように、順方向電流Ｉｆが流れる。

【００１１】この電圧／電流特性を図２に実線で示す。順方向電流Ｉ$_{f}$は図２の第１象現に表されている。上記したチャンネルの形成条件は、第２の半導体領域４の不順物濃度、ゲート絶縁膜６の厚さ、ゲート電極８の種類等の物理定数によって調整可能であり、アノード・カソード間の順方向印加電圧が０Ｖ以上でチャンネルが形成されるよう、その定数を選ぶことにより、図２に示したように順方向電流がほぼ０Ｖから流れる始める特性を実現することができる。

【００１２】具体的には、例えば、第２の半導体領域４をｐ形とする場合には、その半導体領域４（ｐ形）の不純物濃度を５×10^{15}ｃｍ$^{-3}$、ゲート絶縁膜６の厚さを５０ｎｍ、ゲート電極８をｎ形ポリシリコンとする。また、第２の半導体領域４をｎ形とする場合は、その半導体領域４（ｎ形）の不純物濃度を２×10^{15}ｃｍ$^{-3}$、ゲート絶縁膜６の厚さを５０ｎｍ、ゲート電極８をｐ形ポリシリコンとする。このようにすることにより、前記した特性が得られる。

【００１３】かくして、本発明による整流素子は、バリア金属の仕事関数やシリコン表面準位等である順方向電圧が必要なショットキーバリアダイオードよりも、順方向電圧降下を低減できることが、図２により明確化されている。

【００１４】一方、逆方向電圧を印加した場合について図４で説明する。アノード端子１０に対してカソード端子１１よりも低い電圧－Ｅ（逆方向電圧）を印加すると、第２の半導体領域４にはチャンネルは形成されない。すなわち、この第２の半導体領域４は、ＳＯＩ基板を用いた薄いシリコン膜で形成されているので、空乏層が第２の半導体領域４の全域を占め、完全空乏状態となる。これにより、逆方向電圧が印加されても効果的に電流を阻止し、ごく微小なリーク電流Ｉ$_{r}$のみに抑えられる。

【００１５】なお、第２の半導体領域４をｐ形とした場合、この第２の半導体領域４（ｐ形）と第３の半導体領域５（ｎ形）とで形成されるｐｎ接合の障壁によって、完全空乏化しなくても電流の阻止は可能である。しかし、ｐｎ接合にも逆方向のリーク電流は流れるので、上記したように完全空乏化することによって、その電流をより効果的に遮断することができる。

【００１６】図６に、完全空乏化状態となる不純物濃度とシリコン膜厚との関係を、第２の半導体領域４がｐ形の場合について示した。図７には第２の半導体領域４がｎ形の場合について示した。プロットした点は実測データである。本発明による効果を得るためには、第２の半導体領域４の不純物濃度を１×10^{17}ｃｍ$^{-3}$以下製造限界までの範囲の濃度、シリコン膜厚を数百ｎｍ以下製造限界までの範囲の厚みにすれば良いことが分かる。

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【００１７】逆方向電圧／電流特性は、図２に示した第３現象の実線で示した。順方向電圧を低減するほど逆方向電流が増大してしまうショットキーバリアダイオードと異なり、本発明による整流素子は微小な逆方向電流だけであり、整流素子として非常に優れた特性を有する。

【００１８】以上説明したように、従来使用されているショットキーバリアダイオードと比較して、本発明による整流素子は、順方向電流が流れ始める順方向電圧を低減し、低損失化を図ることができることに加えて、逆方向電圧を印加したときの逆方向電流も微小なので逆方向電流による損失も非常に小さいという利点を持っている。順方向電圧降下の低減は、動作電圧の低電圧化が進展するマイクロプロセッサ等用のスイッチング電源の高効率化に大きな利点を有するものである。

【００１９】［その他の実施の形態］なお、本発明の整流素子は、第１の実施の形態で説明した構造のｐ形、ｎ形を反対にした構成を採っても、同様の作用効果が得られることはいうまでもないことである。

【００２０】

【発明の効果】以上から本発明によれば、ＳＯＩ基板上のＭＯＳ構造のゲート電極をアノード端子に接続した構成としたので、順方向電圧の０Ｖから電流が流れ始め、従来から使用されているショットキーバリアダイオードの順方向電圧降下よりも低い順方向電圧降下を実現できる。また、ＳＯＩによる薄いシリコン膜構造のため、逆方向電圧印加時には完全空乏化によりリーク電流を微小ち値に抑えることができる。かくして、本発明の整流素子は、特に低出力電圧のスイッチング電源の整流素子として優れた特性を持ち、スイッチング電源の低損失化に大きな効果を発揮するものである。

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【図面の簡単な説明】

【図１】　本発明の第１の実施の形態を示す整流素子の断面図である。

【図２】　整流素子の電圧／電流特性図である。

【図３】　第１の実施の形態の整流素子の順方向電圧印加時の作用説明図である。

【図４】　第１の実施の形態の整流素子の逆方向電圧印加時の作用説明図である。

【図５】　従来のショットキーバリアダイオードの断面図である。

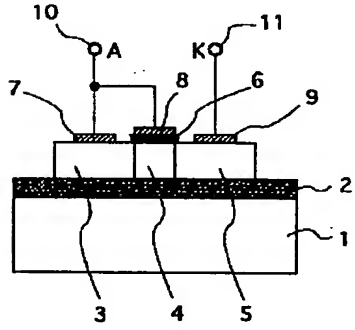
【図６】　第２の半導体領域をｐ形としたときの完全空乏化するシリコン膜厚の不純物濃度の依存性を示す特性図である。

【図７】　第２の半導体領域をｎ形としたときの完全空乏化するシリコン膜厚の不純物濃度の依存性を示す特性図である。

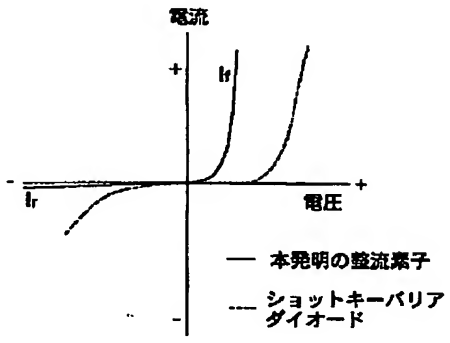
【符号の説明】

１：支持基板、２：埋込み絶縁層、３：第１の半導体領域、４：第２の半導体領域、５：第３の半導体領域、６：ゲート絶縁膜、７：配線用金属層、８：ゲート電極、９：配線用金属層、１０：アノード端子、１１：カソード端子。２１：半導体基板、２２：低濃度の半導体領域、２３：バリア金属、２４、２５：配線用金属層、２６：アノード端子、２７：カソード端子。

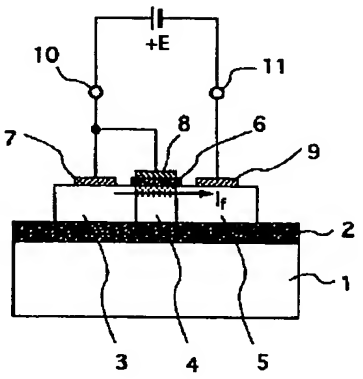
【図１】



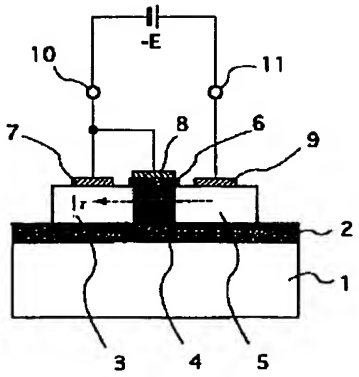
【図２】



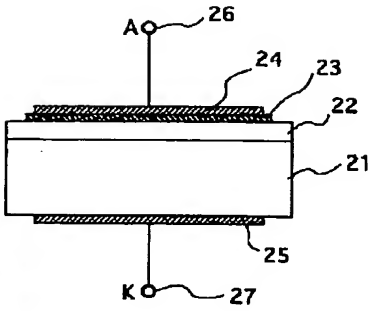
【図３】



【図４】


-E
10
11
7
8
6
9
2
1
3
4
5

【図５】


A
26
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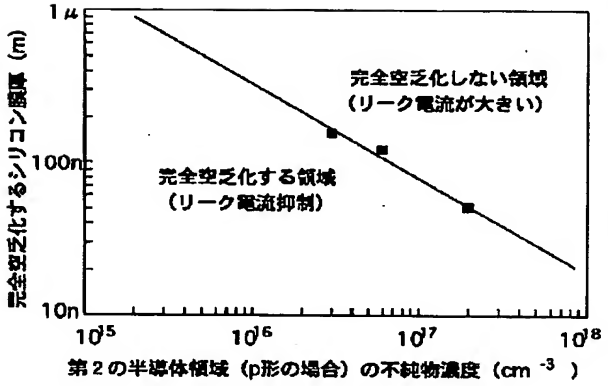
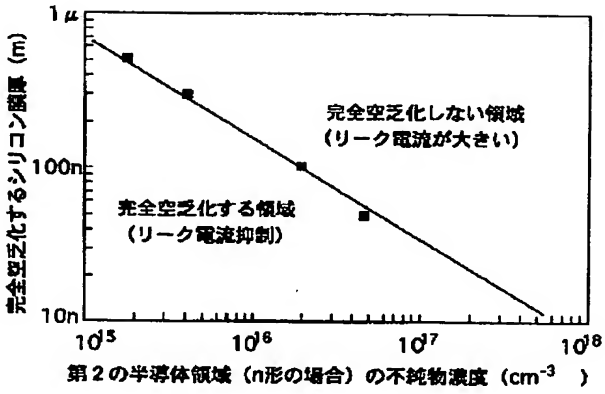
K
27

【図６】


1μ
100n
10n
完全空乏化するシリコン膜厚（m）
完全空乏化しない領域
（リーク電流が大きい）
完全空乏化する領域
（リーク電流抑制）
10^5
10^6
10^7
10^8
第２の半導体領域（p形の場合）の不純物濃度（cm -3 ）

【図７】


1μ
100n
10n
完全空乏化するシリコン膜厚（m）
完全空乏化しない領域
（リーク電流が大きい）
完全空乏化する領域
（リーク電流抑制）
10^5
10^6
10^7
10^8
第２の半導体領域（n形の場合）の不純物濃度（cm-3 ）